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CENTRAL FAX CENTER****APR 23 2007****Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated circuit capable of supporting a plurality of host processor families comprising:

a host processor belonging to a first host processor family;

a reconfigurable processor core coupled to the host processor, the reconfigurable processor core having a first core portion having a first plurality of processors configured to process instructions belonging to the first host processor family and a second core portion having a second plurality of processors configured to process instructions belonging to a second host processor family; and

a processor type select circuit to configure the integrated circuit to process instructions belonging to an instruction set of one of the first or second host processor families ~~family instruction-set~~.

Claim 2 (original): The circuit of claim 1, wherein the first host processor family comprises a processor compatible with an ARM processor family.

Claim 3 (currently amended): The circuit of claim ~~[[1]]~~ 2, wherein the second host processor family comprises a processor compatible with a MIPS processor family.

Claim 4 (previously presented): The circuit of claim 1, further comprising an analog portion integrated on a substrate, the analog portion including:

a cellular radio core;

a radio sniffer coupled to the cellular radio core;

a short-range wireless transceiver core coupled to the cellular radio core; and

a digital portion integrated on the substrate, including the host processor and the reconfigurable processor core.

Claim 5 (previously presented): The circuit of claim 4, wherein the reconfigurable processor core is coupled to the cellular radio core and the short-range wireless transceiver core,

the reconfigurable processor core adapted to handle a plurality of wireless communication protocols.

Claim 6 (previously presented): The circuit of claim 4, further comprising a memory array core coupled to the reconfigurable processor core.

Claim 7 (previously presented): The circuit of claim 5, wherein the plurality of wireless communication protocols includes a Bluetooth™ or IEEE802.11 protocol.

Claim 8 (previously presented): The circuit of claim 5, wherein the plurality of wireless communications protocols includes a Global System for Mobile Communications (GSM) protocol.

Claim 9 (previously presented): The circuit of claim 5, wherein the plurality of wireless communications protocols includes a General Packet Radio Service (GPRS) protocol.

Claim 10 (previously presented): The circuit of claim 5, wherein the plurality of wireless communications protocols includes an Enhance Data Rates for GSM Evolution (Edge) protocol.

Claim 11 (previously presented): The circuit of claim 1, wherein the reconfigurable processor core includes one or more digital signal processors (DSPs).

Claim 12 (previously presented): The circuit of claim 11, wherein the reconfigurable processor core includes one or more reduced instruction set computer (RISC) processors.

Claim 13 (previously presented): The circuit of claim 4, further comprising a router coupled to the host processor, the cellular radio core, and the short-range wireless transceiver core.

Claim 14 (currently amended): The circuit of claim 13, wherein the router further comprises an engine configured to track the destinations of packets and send them in parallel through a plurality of separate pathways.

Claim 15 (previously presented): The circuit of claim 13, wherein the router is configured to send packets in parallel through a primary and secondary communication channel.

Claim 16 (currently amended): A method comprising:

processing a first instruction of a first processor family instruction set in a host processor of a system; and

switching the system to process a first instruction of a second processor family instruction set in a second core portion of a reconfigurable processor core coupled to the host processor, the reconfigurable processor core having a first core portion including a first plurality of processors configured to process instructions belonging to the first processor family instruction set and the second core portion including a second plurality of processors configured to process instructions belonging to the second processor family instruction set; and

switching the system to process a second instruction of the first processor family instruction set after processing the first instruction of the second processor family instruction set.

Claim 17 (cancel)

Claim 18 (previously presented): The method of claim 16, further comprising performing a plurality of wireless protocols using the first processor family instruction set and the second processor family instruction set.

Claim 19 (previously presented): The method of claim 16, wherein the host processor and the reconfigurable processor core are integrated in a single integrated circuit.